

Combined Power Oscillator using GaN HEMT

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Abstract — This paper proposes a new configuration for power oscillator based on the combined power amplifier. The focus is on power combining as a oscillator structure with a positive feedback loop line. The proposed configuration consists of a harmonic-tuned combined power amplifier using two Gallium Nitride High Electron Mobility Transistors (CGH40025), 3dB Wilkinson divider/combiner, a directional coupler, an isolator, a coaxial line and mechanical phase shifters. The steady state oscillation occurs in a delay line feedback loop which length is adjusted to a oscillation frequency. The measured output power and conversion efficiency of the proposed oscillator are 46.8 dBm and 58 %, respectively, at 2.45 GHz with a drain bias voltage of 28 V.

Index Terms — Combined power oscillator, power combining, harmonic-tuned combined power amplifier, GaN HEMT

I. INTRODUCTION

An oscillator is one of the important things for all microwave systems, such as radars, communications, navigations, or electronic warfare. At RF and low microwave frequencies, lumped-element tuning networks are used. All well-known oscillator configurations are good for low power RF and microwave oscillator designs[1]. On the other hand, the vacuum devices have been the only high power RF source used for radar and microwave heating systems that is power oscillator rather than power amplifier[2]. This device still remains in use at kilowatt levels, where solid-state devices cannot compete so far. Nevertheless, the development of high power RF solid-state device technologies may offer an order-of-magnitude improvement in reliability and reduction in size, weight, and low voltage power supply requirements as compared to vacuum devices.

Recently, the advanced technologies of solid-state RF transistors offer good quality with relatively low supply voltages and small size in the systems. On various aspects GaN HEMT is highlighted since that has high breakdown voltage, high electron mobility, high thermal conductivity and low output capacitance to get the high output power and high-efficiency characteristics at high-frequency[3].

The solid-state oscillators with several tens of watt have reported using a single device[2,4], then a simplified circuit can be designed instead of using drive amplifiers which are essential for high-power; the size and cost of system can be decreased as well. However, the output power attainable from a single solid-state device is basically limited by thermal and impedance matching problems. Usually, it is difficult to control matching networks because the output impedance of

the high power transistor is low. Besides, there is the limitation of the ability to generate high output power from a single device.

In this paper, we propose the configuration of the combined power oscillator with harmonic-tuned matching networks for the high power RF sources. The proposed oscillator was designed using a delay-line[5]. A mechanical phase shifter and a variable directional coupler were employed for the oscillation frequency tuning and the power coupling.

II. DESIGN OF HIGH-EFFICIENCY POWER AMPLIFIER AND OSCILLATOR

A. Implementation of Harmonic-tuned Combined Power Amplifier

A power amplifier with a high efficiency can be obtained by adjusting the output impedances at fundamental and harmonic frequencies. Generally, the voltage and current waveforms of the harmonic-tuned amplifier control at the transistor output to obtain the maximum efficiency.

First, the single high-efficiency power amplifier with a harmonic-tuned matching networks was designed before balanced amplifier is designed. The transistor used in this design is a 25W GaN HEMT(CGH40025) from Cree and the Agilent Advanced Design System (ADS) simulation code was used. Using load-pull simulation with a non-linear model provided by Cree at 2.45 GHz the optimum load impedances were found for a DC drain voltage of 28 V and the gate voltage of -2.19 V. Fig.1 shows the simulated results of the harmonic impedances of the output harmonic-tuned matching network. The optimum load impedances of fundamental, 2nd harmonic and 3rd harmonic frequency are 7.892-j0.625, 50.59+j52.92 and 1.57+ j57.15, respectively.

Based on the simulation results, the output harmonic-tuned matching network of the power amplifier was designed. And the input matching network matched by conjugate matching for maximum power transfer. The designed harmonic-tuned amplifier was fabricated on TACONIC TLX-7 ($\epsilon_r=2.6$ $\tan\delta=0.0019$, $h=0.504\text{mm}$). Fig. 2 shows the measured results of an output power, a power gain, and a drain efficiency of the fabricated amplifier with a drain bias voltage of 28 V and a gate bias voltage of -3.3 V as a function of input power. As shown in Fig. 2, the output power is 44.3 dBm, the drain efficiency is 73.9 % and the gain is 10.2 dB.

Another power amplifier was also fabricated with same conditions for the combined oscillator.

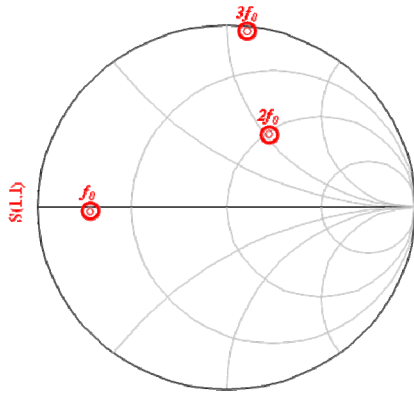


Fig. 1. Simulated results of the harmonic impedance of the output harmonic-tuned matching network.

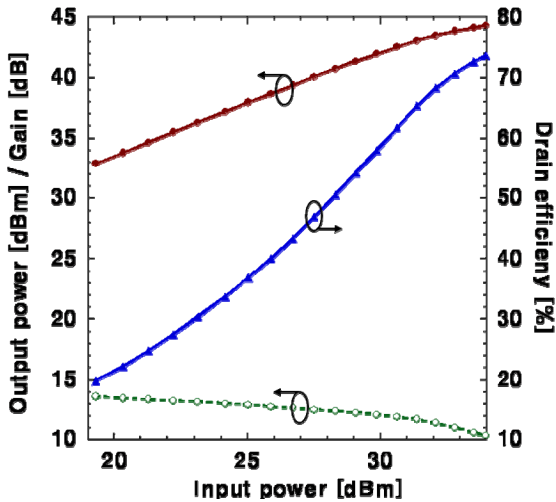


Fig. 2. Measured results of fabricated amplifier as a function of input power.

The measured results of an output power, a drain efficiency and power gain with a drain bias voltage of 28 V and a gate bias voltage of -3.1 V were 44.7 dBm, 70.1 % and 10.3 dB, respectively.

Finally, a harmonic-tuned balanced power amplifier with 3 dB Wilkinson divider/combiner was fabricated and measured. Fig. 3. shows the photograph of the fabricated balanced power amplifier. When the balanced amplifier measured, the gate bias voltage fed each due to the difference between the characteristic of the transistors. Fig. 4 shows the measured results of an output power, a drain efficiency and power gain of the balanced power amplifier. As shown in Fig. 4, the output power is 47.9 dBm, the drain efficiency is 67 % and the power gain is 11.1 dB.

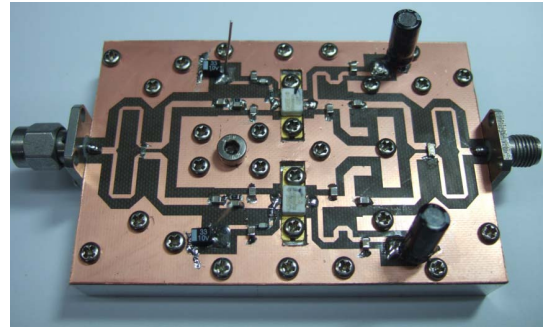


Fig. 3. Photograph of the fabricated balanced power amplifier.

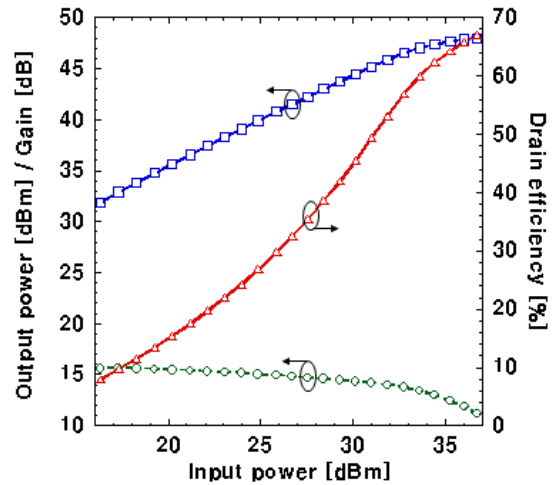


Fig. 4. Measured of the fabricated balanced power amplifier

B. Implementation of Combined Power Oscillator

The schematic of designed combined power oscillator is shown Fig. 5. This circuit is designed due to a limitation of the output power from a single amplifier. So, we propose the combined power oscillator using balanced power amplifier in this paper. The delay-line structure used for high power oscillator[5]. A positive-feedback oscillator enables the output power of the transistor to feedback to the input of the transistor through coupling capacitor. The oscillation frequency is decided by the phase of feedback loop line and output power in normal status is decided by the saturation power of the amplifier. In other words, an oscillation occurs at the frequency when the phase of feedback loop satisfies '0' and then the output power is kept at the saturation power of the transistor.

The proposed RF oscillator was designed experimentally by using the balanced power amplifier. The positive-feedback loop was composed of a directional coupler, coaxial cables, an isolator and a mechanical phase shifter. First of all, the phase of feedback loop was adjusted by using the coaxial cables and

mechanical phase shifters. The output power was controlled that was coupling into the feedback loop by using the directional coupler. To get the same results as the output power and drain efficiency from the balanced power amplifier, the coupling factor has to be same value as the gain of the balanced power amplifier. The measured level of coupling by the directional coupler when the oscillation occurs was 9.7 dB and the power gain of the fabricated balanced power amplifier was 11.1 dB. The difference of 1.4 dB is due to the insertion loss of passive components.

The configuration of the oscillator measurement is shown in Fig 5. As it is shown, the output power of the balanced power amplifier is coupled to the feedback loop through a directional coupler in this circuit. The phase shifter and coaxial lines control phase to occur oscillation in expected frequency. An isolator was used to prevent the mismatching of an input impedance by the feedback loop.

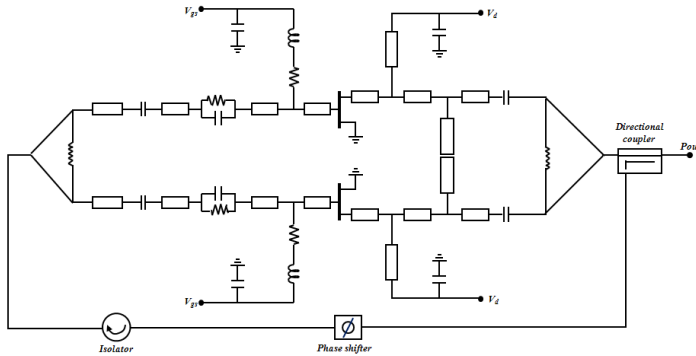


Fig. 5. Schematic of designed combined power oscillator.

III. EXPERIMENTAL RESULTS

Fig. 6. shows the photograph of the measurement setup for oscillation test. This oscillation test was carried out using a balanced power amplifier. Fig. 7(a) shows the output spectrum of the oscillator at 2.45 GHz, Fig. 7(b) shows the results of phase noise at 1 KHz, 10 KHz, 100 KHz and 1 MHz offset. The output spectrum and phase noise were measured by Agilent performance spectrum analyzer (PSA) E4440 in the range of 470 kHz of RBW and 50 MHz span. As shown in Fig.

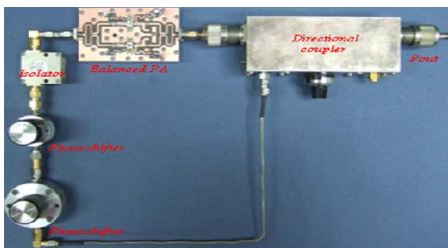
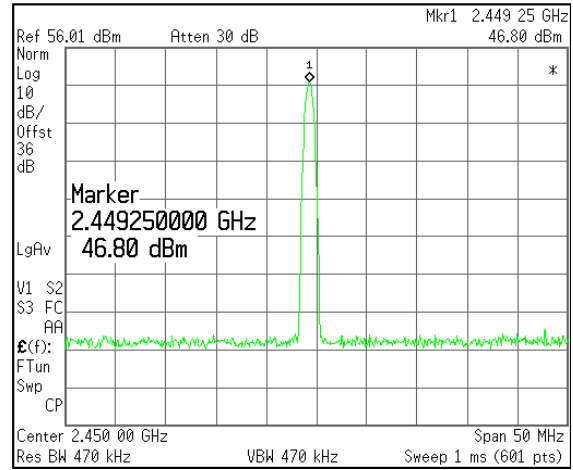
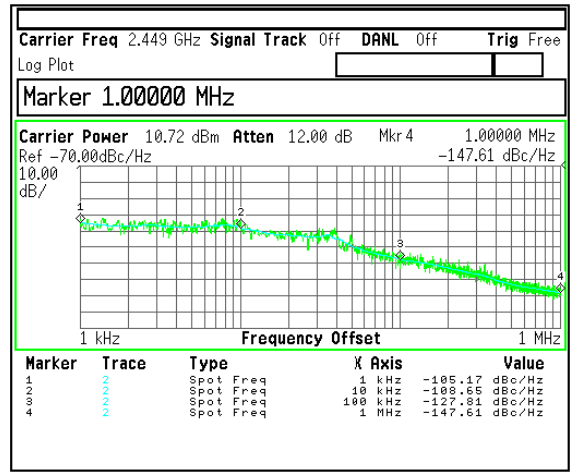


Fig. 6. Photograph of the measurement setup for oscillation

7(a), 46.8 dBm of the output power and 58 % of conversion efficiency with drain bias voltage of 28 V and in Fig. 7(b), -106.17 dBc/Hz, -108.65 dBc/Hz, -127.81 dBc/Hz and -147.61 dBc/Hz at 1kHz, 10kHz, 100kHz and 1MHz offset frequency, respectively. The output power resulted from the combined power oscillator measurement was 46.8 dBm, which was 1.1 dB less than previous balanced power amplifier measurement. The main cause of power loss is due to the insertion loss of directional coupler for coupling into feedback line.



(a)



(b)

Fig. 7. Measured results (a) output spectrum (b) phase noise

IV. CONCLUSION

In this paper, we propose a new configuration of the combined power oscillator for high RF power source. First, the high-efficiency power amplifier with harmonic-tuned matching network was designed and fabricated using GaN HEMT. The amplifiers has the output power of 44.3 dBm, 44.7 dBm and the drain efficiency of 73.9 %, 70.1 % at 2.45 GHz. Then, the balanced power amplifier using 3dB

Wilkinson divider/combiner was designed and fabricated. The measured results were the output power of 47.9 dBm and conversion efficiency of 67% with a drain bias voltage of 28 V. Finally, the combined power oscillator using the fabricated balanced power amplifier was experimentally measured. The output power of 46.8 dBm and conversion efficiency of 58% at 2.45 GHz. These results are compared with those of other power oscillators in Table I. The proposed configuration using the combined power amplifier for high RF power oscillator has been experimentally validated. Higher power can be realized by configuring power FETs of more than two in parallel.

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TABLE I
 PERFORMANCE COMPARISON OF PUBLISHED
 POWER OSCILLATORS

Frequency	Output power	Efficiency	Reference
2 MHz	3 W	95 %	[6]
410 MHz	75 W	67 %	[4]
916 MHz	29 W	64.5 %	[7]
981 MHz	6.5 W	73 %	[5]
1.6 GHz	0.25 W	67 %	[8]
2.45 GHz	47.9 W	58 %	This work
4.4 GHz	0.004 W	43 %	[9]
5 GHz	0.3 W	59 %	[10]

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